Design, Fabrication and Characterization of High-Performance Silicon Nanowire Transistors

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***Abstract*-We report the fabrication and characterization of double-gated Si nanowire field effect transistors with excellent current-voltage characteristics, low subthreshold slope ~ 85 mV/dec and high on/off current ratio ~ 10^6. The Si nanowire devices are fabricated by using a self-aligned technique with standard photolithographic alignment and metal lift-off processes, enabling the large-scale integration of high-performance nanowire devices. We have also studied the effect of device structure and forming gas rapid thermal annealing on the nanowire transistor's electrical properties. We conclude that the self-aligned fabrication and non-overlapped gate-source/drain structure combined with appropriate post annealing leads to the excellent observed device performance.**

I. Introduction

Semiconductor nanowires have been of great interest as an important active medium for applications in nanoelectronics. Nanowire field effect transistors (NW FETs), one of the key devices in nanoelectronics, have been demonstrated recently with improving performance (e.g., subthreshold slope from 1000s to 100s mV/dec). The ultimate device electrical properties strongly depend on the device structure and interface quality and are directly affected by fabrication processes. Most of the current research on self-assembled nanowire devices involves harvesting nanowires from the preparation substrate, and suspending them in liquid to form a nanowire solution before the manipulation by using fluidic alignment [1], dielectrophoresis [2] or nanoscale probe methods [3, 4]. Such processes will introduce debris, particles and other unknown materials surrounding the nanowires and will contaminate their surface. Some other research used electron beam microscopy to examine the nanowire's position during the nanowire alignment, which introduced additional source of contamination. Importantly, the effectiveness of cleaning the nanowire after such manipulations is very limited because one needs to avoid losing the nanowires, which attach on the surface weakly via electrostatic force. Therefore, the nanowire surface will be left contaminated when the device is made. Such a contaminated surface will dramatically increase the nanowire device interface states (D_{it}), which can seriously deteriorate the device performance, such as the transistor subthreshold slope.

In this paper we introduce a self-aligned technology to fabricate large numbers of high-performance nanowire devices. During the fabrication processes, the nanowires are grown from pre-defined catalysts. The source/drain and gate electrodes are aligned and patterned via conventional photolithography. We fabricated various nanowire devices, including Si nanowire (SiNW) FETs, by using this technique. As a representative examples, the SiNW FETs with high-k dielectric fabricated by using this technology show high electrical performance: large on/off current ratio ~10^6 and sharp subthreshold slope ~ 85 mV/dec, which is better than current recently reported values [5, 6]. In this work we have also investigated the effect of device structure and annealing conditions on the SiNW FET's electrical characteristics. We attribute the device performance improvement to the low surface contamination, appropriate annealing processes and the self-aligned nature of the device structure.

II. Experimental

The "self-alignment" processes by which these devices are fabricated are shown in Fig. 1. The key steps in this fabrication

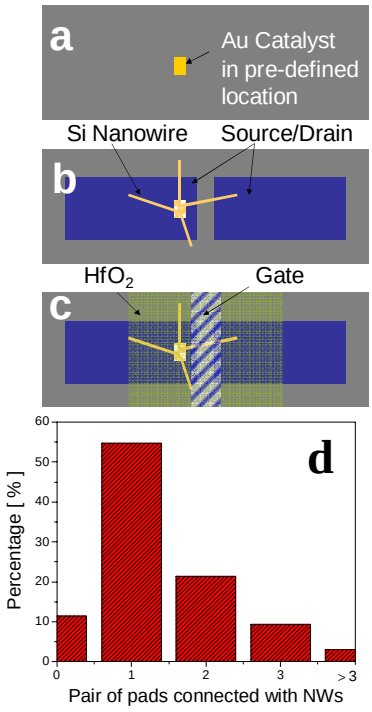

Fig. 1 Schematics of self-alignment fabrication processes are shown in (a): Au catalyst is patterned on SiO_2, (b): SiNW is grown from the Au catalyst, oxidized and aligned with source/drain contacts, and (c): HfO_2 and top gate are patterned on the SiNW. (d): The percentage of FETs which Source and Drain electrodes are connected with 0, 1 or more nanowires. The distance between Source and Drain electrodes is from 3 µm to 8 µm.

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process are self-assembling and patterning the SiNWs grown from Au catalyst on pre-defined locations. First, a 50 nm thermal SiO_2 was thermally grown on p-type silicon substrates as the insulator of the bottom gate. Then a Au film (~ 1 nm) was patterned on the oxide surface as the SiNW growth catalyst by using photolithography and metal lift-off processes (see Fig. 1 (a)). The SiNWs were grown in a low temperature chemical vapor deposition furnace, at 420° C, under 500 mTorr SiH_4 via a vapor-liquid-solid mechanism [7, 8]. SiNWs of ~ 20 nm in diameter and 20 µm ~ 30 µm in length were obtained.

We then thermally oxidized the SiNWs at 700 °C for 30 minutes. Based on the work on SiNW oxidation [9], a thin layer of oxide (1 nm ~ 2 nm) grows on the SiNW surface, which improves the interface between the SiNW and the subsequently deposited HfO_2 layer. The following compatible fabrication processes were used to pattern the metal contacts (i.e. source, drain and top gate electrode) on the SiNWs. First we spin the lift-off resist (LOR) and photoresist (PR) on the substrate (with nanowires) and define the patterns for the source and drain contacts of SiNW FET with photolithographic processes (see Fig. 1 (b)). This is followed by a wet etch for 2 minutes with 2% HF to remove the oxide from the SiNWs and a layer of Al is deposited by thermal evaporation and defined by metal lift-off to form the Source and Drain electrodes. A layer of HfO_2 (~ 25 nm) is then deposited as the top gate dielectric of the SiNW FET by atomic layer deposition at 250 °C. The top gate electrode (Al) is formed by using similar processes with the formation of source and drain electrodes (see Fig. 1 (c)). Finally, the resulting SiNW FET was annealed in ambient forming gas (5% H_2 in N_2) at 380 °C for 15 minutes by using a rapid thermal annealing tool. This step is critical for achieving better electrical performance due to the following two reasons: (1) the forming gas annealing can greatly reduce D_{it}; (2) the contact between the Al metal to the SiNW and HfO_2 will be improved. The Al in the Source/Drain regions forms Schottky barrier contacts to the SiNWs. Figures 1 (d) shows the percentage of pairs of metal pads connected with one or more nanowires. By tuning the amount of Au catalyst, device structure and nanowire length, about 90% of the pre-defined locations successfully form the expected SiNW devices with one or more nanowires connected.

III. RESULTS AND DISCUSSION

The schematic device cross-section and scanning electron microscope (SEM) images of typical SiNW FETs with 1- µm and 0-µm gate to source/drain overlap (ΔL) are shown in Figures 2 (a), (b) and (c). Because the source and drain consist of Schottky junctions between the Al contacts and the intrinsic SiNW, the SiNW FET is expected to have Schottky-barrier PMOSFET characteristics [10, 11].

Typical I-V characteristics recorded from a SiNW FET fabricated by the self-aligned technique described above, with gate length L = 3 µm and gate overlap ΔL = 0 µm (see Fig. 2 (c)) are shown in Figures 3 (a) and (b). In Fig. 3 (a), the drain to source current (I_{DS}) vs. drain to source voltage (V_{DS}) curves for several gate to substrate voltage (V_{GB}) values show

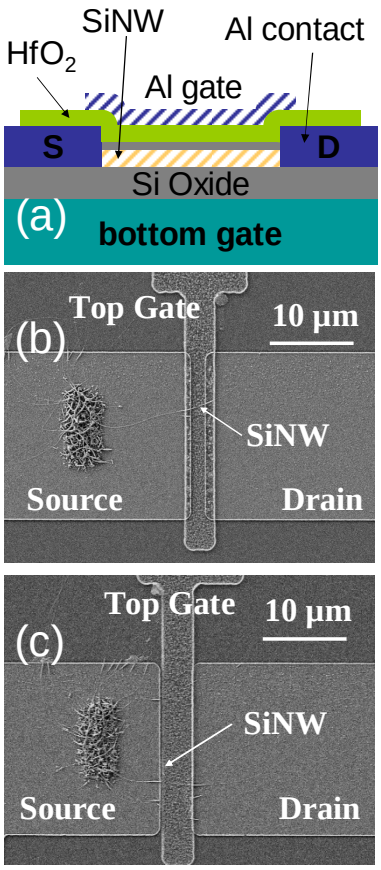

Fig. 2 (a) Schematic of a SiNW FET with HfO_2/SiO_2 as the gate dielectric. (b) and (c) are the scanning electron microscopic images of SiNW FETs with and without 1 µm Gate-Source/Drain overlap, respectively.

that I_{DS} first increases and then saturates with increasing negative V_{DS} and I_{DS} increases with increasing negative V_{GB}, similar to a conventional PMOSFET. Thus, the SiNW FET is indeed a p-channel FET as expected. The transfer curves I_{DS}-V_{GB} with V_{DS} = - 50 mV (Fig. 3 (b)) show a large on/off current ratio ~ 10^6, low off current ~ 10^{-15} A, and sharp subthreshold slope $S = d(V_{GB})/d(\mathrm{Log}(I_{DS}))$ = ~ 85 mV/dec. The subthreshold slope, a parameter indicating how fast a transistor can switch, is directly extracted from the I-V transfer curve. This evaluation of the device switching speed is more accurate than the evaluation based on the conductivity and mobility characteristics of the devices, as these characteristics are indirectly calculated from the geometry and specific material parameters and may introduce errors. Therefore, the performance of different NW FETs is best compared on the basis of their respective subthreshold slope. The SiNW FETs demonstrated in this work have better subthreshold slope, compared to the recent values (104 ~ 140 mV/dec) [5, 6]. We believe the improvement is due to a lower interface state density (D_{it}) between the dielectric and the SiNW, achieved by the self-aligned process used for the fabrication. In addition, compared to device with Ni-Si source and drain contacts, [5, 6] our SiNW FETs showed low off current, partially because the Al / intrinsic Si Schottky contact has higher barrier to more effectively suppress electron conduction [10, 11].

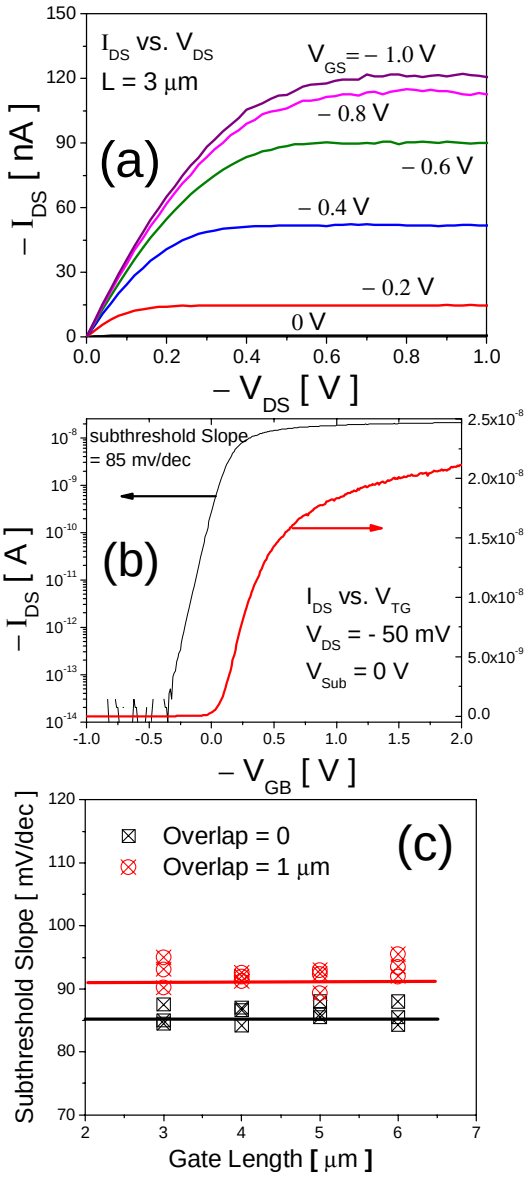

Fig. 3 (a) I_{DS}-V_{DS} curves at V_{GB} = 0 V to -1 V in - 0.2 V steps. (b) I_{DS}-V_{GB} curves with V_{DS} = - 50 mV at linear- and log-scale of a SiNW FET with one nanowire, L = 3 μm and ΔL = 0, showing S = 85 mV/dec. (c) Average subthreshold slope of overlap and non-overlap Si NW FETs with different gate length, L = 3 μm ~ 6 μm. Line is a guide for the eyes.

As shown in Fig. 3 (c), we have also investigated the effect of device geometry on the subthreshold slope: SiNW FETs with zero overlap (ΔL = 0 μm) have a slightly sharper subthreshold slope (S = 85 mV/dec) than those with ΔL = 1 μm (S = 90 mV/dec), based on the average of more than twenty FETs with L = 3 ~ 6 μm. This difference results from the parasitic impedance (i.e., series resistance) of the overlap region between gate and source/drain [12, 13]. In addition, these data illustrate the good reproducibility of the simultaneous, batch fabrication of our self-aligned process.

Rapid thermal annealing (RTA) in forming gas at 380 °C is a very helpful step to decrease D_{it}. Un-annealed SiNW FETs show an average subthreshold slope of ~ 180 mV/dec. The I_{DS}-V_{GB} curves of the annealed and un-annealed SiNW FETs in the

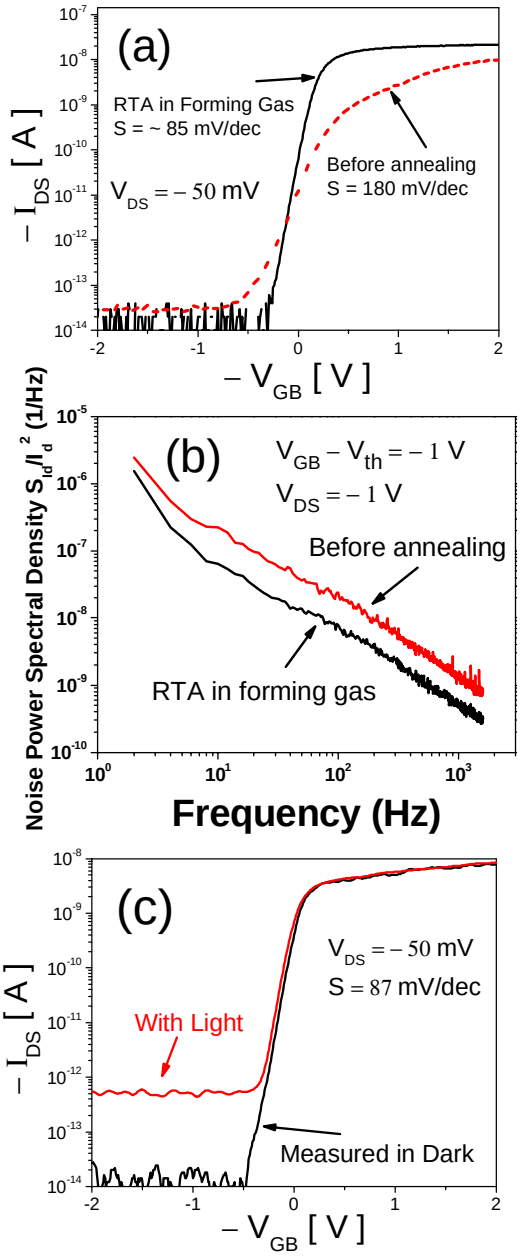

Fig. 4 (a) The I_{DS}-V_{GB} curves of a typical SiNW FET before annealing and after rapid thermal annealing in forming gas at 380 °C for 15 minutes. (b) Noise power spectral density as a function of frequency for a SiNW FET before and after annealing. (c) The I_{DS}-V_{GB} curves of a typical SiNW FET measured with and without light. Light increases the off-state current but has no effect on the subthreshold slope (~ 87 mV/dec).

subthreshold region are compared in Fig. 4 (a). The subthreshold slope can be simply expressed as

$$S = 2.3 \cdot \Phi_t \cdot \left(\frac{C_{OX} + C_{it}}{C_{OX}}\right) \qquad (1)$$

where Φ_t (= kT/q) is the thermal potential (~ 26 mV at room temperature), C_{OX} is the equivalent gate oxide capacitance, and C_{it} is the capacitance corresponding to the interface state density (D_{it}). The subthreshold slope is improved from 180 mV/dec to 85 mV/dec by rapid thermal annealing in forming

gas. From the Eq. (1), this corresponds to an interface state density reduction of ~ 83% by the annealing. In addition, the SiNW-FET 1/f noise characteristics in Fig. 4 (b) show that the noise magnitude significantly decreased after RTA in forming gas. Generally larger noise power spectral density corresponds to larger D_{it}. The noise measurement indicates the D_{it} decreases after annealing, which is in agreement with the subthreshold-slope analysis. Fig. 4 (c) showed the I_{DS}-V_{GB} characteristics of a typical high-performance SiNW FET measured with and without white light. The light increases the transistor off-state current by photoelectric generation in the SiNW. But the light has no significant effect on the transistor threshold voltage and subthreshold slope. This indicates the amount of interface state activated by light is insignificant to affect the high performance of the SiNW FET prepared by the self-alignment approach.

IV. Conclusions

In conclusion, we have developed a self-aligned technique to fabricate high-performance SiNW FETs. The rapid thermal annealing in forming gas is shown to significantly reduce the interface state density of the device and improve subthreshold slope, and it is thus a key component of our technique. Moreover, the device's subthreshold slope has also been shown to be affected by the gate-source/drain overlap. These devices have large on/off current ratio, low off-state current and good subthreshold: ~ 85 mV/dec, a considerable improvement from previously reported results. The excellent performance is attributed to the clean fabrication technique, annealing process and details of the device configuration.

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